process according to the present invention, hard passivation layer 155 includes silicon nitride. Silicon nitride hard passivation layer 155 contains nitrogen (N), the same chemical element found in nitrous oxide gas 145. Hard passivation layer 155 is conformally deposited over the above-mentioned structures to a thickness of about $1\mu m$ or less. Soft passivation layer 160 is then deposited on hard passivation layer 155. Soft passivation layer 160 may also be deposited by PECVD. In one embodiment of the process according to the present invention, soft passivation layer 160 is a photodefinable polyimide layer spun to a thickness of approximately 11.5 μm, which reduces to a thickness of approximately 3 μm at the end of processing.

On page 17, starting on line 12, please amend the paragraph as follows:

Once soft passivation layer 160 is cured, the exposed hard passivation layer 155 is etched to form openings to bond pads 110 and 115 and to remove hard passivation layer material from scribe street area 140. Adhesion layer 150 is also removed in these areas. In the embodiment where hard passivation layer 155 includes silicon nitride and adhesion layer 150 includes silicon oxynitride, a plasma etch process that removes both silicon oxynitride and silicon nitride is performed. In the case where the integrated circuits include a multi-layer conductive material such as the TiN ARC layer described above, this material may be removed at this step. A typical etchant that may etch silicon oxynitride, silicon nitride, and the TiN ARC layer may include for example, a NF_3/He and SF_6/He.

On page 19, starting on line 18, please amend the paragraph as follows:

Figures 16-18 illustrate cross-sectional views through the portions of the integrated circuits in connection with the process described in connection with **Figures 9-15** for use with a C4 platform integrated circuit devices 200 and 205. In **Figure 16,** integrated circuit devices 200 and 205 are separated by a scribe street area 240. Integrated circuit devices 200 and 205 include conductive material bond pads 210 and 215, respectively, and guard rings 220 and 225, respectively. Scribe street area 240 contains E-Test pad 230. Adjacent the top surface of oxide layer 28 is an adhesion layer 250 of silicon oxynitride, for example. Overlying the conductive structures of the wafer

B3

is hard passivation layer 255 of silicon nitride, for example. In one embodiment, the silicon oxynitride layer is formed by exposing oxide layer 28 of silicon dioxide to a nitrous oxide (N_2O) treatment. Overlying hard passivation layer 255 is soft passivation layer 260 of photodefinable polyimide, for example. For a more detailed description of the formation of hard passivation layer 255, soft passivation layer 260, and adhesion layer 250, reference is made to **Figures 9-12** and the accompanying text.

On page 21, starting on line 12, please amend the paragraph as follows:

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Figure 20 illustrates a portion of a semiconductor device with spacers formed thereon. Spacers 408 are formed along the sidewalls of a hardmask 406 and a gate 404 of a Complementary Metal Oxide Semiconductor (CMOS), for example. Spacers 408 are passivated in an oxide layer 410, an adhesion layer 412, and a passivation layer 414 in accordance with an embodiment of the present invention. Spacer formation is well-known in the art. Spacers 408 are typically made of silicon nitride. However, it should be appreciated by those of ordinary skill in the art that spacers 408 may be made from other dielectric materials and may include a single dielectric layer, such as silicon dioxide, or several layers formed by various methods. In one embodiment, each spacer 408 is comprised of oxide layer 410 of silicon dioxide. An adhesion layer 412 of silicon oxynitride is formed when the silicon dioxide layer is exposed to a plasma treatment of nitrous oxide gas. In the embodiment described above, a passivation layer 414 made of silicon nitride, for example, is formed over adhesion layer 412, resulting in a strong chemical bond between oxide layer 410 and passivation layer 414. Gate 404 is separated from substrate 400 by intermediate layer 402.

IN THE CLAIMS

Please amend the claims as follows:

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17. (Amended) An integrated circuit (IC) comprising:
an oxide layer;
an adhesion ~~layer~~ formed over said oxide layer; and